AP-99-002B

October 6, 2003

To: Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572
28 Davis Avenue
Poughkeepsie, N.Y. 12603

Subject: Serial No. 10/616,751 07/10/03

Peter Lee et al.

A STACKED GATE FLASH MEMORY CELL WITH REDUCED DISTURB CONDITIONS

Grp. Art Unit:

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56. Copies of each document is included herewith.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on October 10, 2003.

Stephen B. Ackerman, Reg.# 37761

Signature/Date Stephen B. Ackerman 10/10/03

U.S. Patent 5,880,991 to Hsu et al., "Structure for Low Cost Mixed Memory Integration, New NVRAM Structure, and Process for Forming the Mixed Memory and NVRAM Structure", describes an integration of a flash EEPROM with a DRAM and an SRAM on the same chip.

U.S. Patent 5,654,917 to Ogura et al., "Process for Making and Programming a Flash Memory Array", describes a process for fabricating a flash memory array. The embedded structure of the flash memory cells are used in a Domino and Skippy Domino schemes to program and read the cells.

U.S. Patent 5,479,036 to Hong, "Fieldless Split-Gate EPROM/Flash EPROM", describes a structure and process for a split gate flash memory cell. The process utilizes self aligned techniques to produce an array of flash memory cells.

U.S. Patent 5,172,200 to Muragishi et al., "MOS Memory Device Having a LDD Structure and a Visor-Like Insulating Layer", describes an EEPROM flash memory cell which utilizes a lightly doped drain structure for both the drain and the source.

U.S. Patent 5,168,465 to Harari, "Highly Compact EPROM and Flash EEPROM Devices", describes a split channel and other cell configurations which are used to produce an EEPROM. The elements of the EEPROM are produced using a cooperative process of manufacture to provide self alignment. A programming technique allows each memory cell to store more than one bit of information.

Sincerely,

Stephen B. Ackerman,
Reg. No. 37761

Form PTO-1449

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(use several sheets if necessary)

Docket Number (Optional)	Application Number
AP-99-002B	10/616,751
Applicant: Peter Lee et al.	
Filing Date: 07/10/03	Group Art Unit:

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	5880991	3/9/99	Hsu et al.	365	182	4/14/97
	5654917	8/5/97	Ogura et al.	365	185.18	5/14/96
	5479036	12/26/95	Hong	257	315	1/11/95
	5172200	12/15/92	Muragishi et al.	257	315	1/4/91
	5168465	12/1/92	Harari	257	320	1/15/91

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.